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EXAMINER	
GANDHI, DIPAKKUMAR B	
ART UNIT	PAPER NUMBER
2117	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/519,346	DE WINTER, RUDI	
	Examiner	Art Unit	
	DIPAKKUMAR GANDHI	2117	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 April 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 December 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Response to Amendment

1. The amendment filed on 04/01/2008 has been entered.

2. The amendments to the abstract, specification and a Supplemental Application Data Sheet filed on 04/01/2008 are accepted.

3. Applicant's arguments have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claim 1 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The claim 1 recites, "if the external test circuitry is free from maintaining the integrated circuit in a test mode...". However the claim 1 does not recite the other condition, "if the external test circuitry is not free from maintaining the integrated circuit in a test mode...". Thus claim 1 recites only one condition and not the other condition.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

8. Claims 1, 2, 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Toyofuku et al. (JP 57-133656) in view of Ishikawa (US 4,638,247).

As per claim 1, Toyofuku et al. teach an integrated circuit comprises one or more integrated circuit elements and one or more input/output pins, the one or more integrated circuit elements including an interface element for interfacing with external test circuitry, the interface element communicating with the external test circuitry via a single input/output pin dedicated for testing wherein the single pin connected operates with several logic thresholds (abstract, Toyofuku et al.)

However Toyofuku et al. do not explicitly teach specifically that if the external test circuitry is free from maintaining the integrated circuit in a test mode for a predetermined period, the integrated circuit defaults from the test mode to a normal mode.

Ishikawa in an analogous art teaches an integrated circuit comprising a drive control circuit operative to produce normal drive control signals in the absence of said test signal (col. 4, lines 50-57, Ishikawa).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Toyofuku et al.'s patent application with the teachings of Ishikawa by including additionally that if the external test circuitry is free from maintaining the integrated circuit in a test mode for a predetermined period, the integrated circuit defaults from the test mode to a normal mode.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity for the integrated circuit to return to normal mode without sending additional signal from the external circuitry.

- As per claim 2, Toyofuku et al. and Ishikawa teach the additional limitations.

Toyofuku et al. teach that the interface element is embedded into the integrated circuit as a single pin interface between the digital integrated circuit and the external test circuitry (abstract, Toyofuku et al.).

- As per claim 5, Toyofuku et al. and Ishikawa teach the additional limitations.

Toyofuku et al. teach that a "pad detection" detector determines whether there is a connection with an external tester or other external circuitry by assessing the voltage on the single pin (abstract, Toyofuku et al.).

9. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Toyofuku et al. (JP 57-133656) and Ishikawa (US 4,638,247) as applied to claim 2 above, and further in view of Stewart et al. (US 4,947,357).

As per claim 3, Toyofuku et al. and Ishikawa substantially teach the claimed invention described in claim 2 (as rejected above).

However Toyofuku et al. and Ishikawa do not explicitly teach specifically that the interface element receives test data and commands from the external test circuitry in response to which a crash block controls and commands scan path elements within the digital integrated circuit and returns the resulting data to the external test circuitry.

Stewart et al. in an analogous art teach that in a fifth aspect, the invention features a method of testing an integrated circuit with an external testing device, the integrated circuit having a first scan chain disposed between pads and functional circuitry of the integrated circuit, and the functional circuitry having a second scan chain disposed therein, the method comprising the steps of: (a) scanning an internal test data word from the testing device into the second scan chain to apply the internal test data word to the functional circuitry; (b) applying an external test data word from the testing device to a portion of the pads corresponding to inputs of the functional circuitry; (c) opening a portion of the first scan chain corresponding to the input pads to couple the external test data word through the input portion of the first scan chain and apply the external test data word to the inputs of the functional circuitry; (d) coupling outputs produced by the functional circuitry in response to the internal and external test data words through a portion of the first scan chain to pads corresponding to the outputs of the functional circuitry for receipt by the testing device; (e) closing the input portion of the first scan chain to decouple the input pads from the inputs of the functional circuitry; (f) advancing the state of the functional circuitry after the input portion of the first scan chain has been closed to cause the functional circuitry to generate result data based on the internal and external test data words, the result data being loaded in the second scan chain;

and (g) scanning the result data from the second scan chain to the testing device for evaluation (col. 6, lines 18-47, Stewart et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Toyofuku et al.'s patent application with the teachings of Stewart et al. by including additionally that the interface element receives test data and commands from the external test circuitry in response to which a crash block controls and commands scan path elements within the digital integrated circuit and returns the resulting data to the external test circuitry.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to test the integrated circuit using test data and commands from the external test circuitry.

10. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Toyofuku et al. (JP 57-133656) and Ishikawa (US 4,638,247) as applied to claim 1 above, and further in view of Davies, Jr. (US 4,449,065).

As per claim 4, Toyofuku et al. and Ishikawa substantially teach the claimed invention described in claim 1 (as rejected above).

However Toyofuku et al. and Ishikawa do not explicitly teach specifically that the logic thresholds define several logic levels, which enable data and timing signals to be differentiated on a single pin.

Davies, Jr. in an analogous art teaches that a simple six-transistor input buffer for generating and applying binary function test signals to associated circuitry in an integrated circuit package.

The buffer recognizes three different voltage levels of an input signal that is applied to a single input test pin and generates three corresponding binary output signals that may be used for testing various functions of the associated circuitry (abstract, Davies, Jr.). Davies, Jr. teaches that the tri-level input buffer circuit includes first and second branch circuits connected between a drain voltage source and ground reference. Each branch circuit includes a CMOS transistor pair in series with a transistor switch and an output from each branch circuit is taken from the interconnection of the p-channel field effect transistor and the n-channel transistor forming a CMOS pair. Each branch circuit is initialized by the application of a pre-charge pulse from the chip system clock followed thereafter by an evaluate pulse. If the applied

input signal is at the "one" level, both branch outputs are low. If the applied input is at the low "zero" level, both outputs are high. However, if the applied input voltage level is within the threshold range of both n-channel and p-channel transistors and so that both of these transistors are conductive, one branch circuit will produce an output of "0" while the other branch will output a "1" (col. 1, lines 29-47, Davies, Jr.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Toyofuku et al.'s patent application with the teachings of Davies, Jr. by including additionally that the logic thresholds define several logic levels, which enable data and timing signals to be differentiated on a single pin.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to apply signals with different logic levels to the integrated circuit on a single pin and test the integrated circuit.

11. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Toyofuku et al. (JP 57-133656) and Ishikawa (US 4,638,247) as applied to claim 1 above, and further in view of Wise et al. (US 5,404,304).

As per claim 6, Toyofuku et al. and Ishikawa substantially teach the claimed invention described in claim 1 (as rejected above).

However Toyofuku et al. and Ishikawa do not explicitly teach specifically that if a voltage on the single pin is held at a voltage below "low" for a period of time determined by an "escape 0 timer" then the integrated circuit will decide there is no tester connected to the single pin.

Wise et al. in an analogous art teach that when the high lead voltage goes above the comparator 98 threshold and the low lead voltage goes below the comparator 100 threshold, both comparators turn on to send an open indication to the fault timing circuit 36 via AND gate 102 and the timeout period begins. If the timeout expires an open circuit fault is latched (col. 5, lines 33-38, Wise et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Toyofuku et al.'s patent application with the teachings of Wise et al. by including

additionally that if a voltage on the single pin is held at a voltage below "low" for a period of time determined by an "escape 0 timer" then the integrated circuit will decide there is no tester connected to the single pin.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity for the integrated circuit to return to normal mode without sending additional signal from the external circuitry.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DIPAKKUMAR GANDHI whose telephone number is (571)272-3822. The examiner can normally be reached on 9:00 AM - 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jacques Louis-Jacques can be reached on (571) 272-6962. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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